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6. AUTHOR(S)
Vincent P. Heuring

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of Colorado at Boulder
Optoelectronic Computing Systems Center and
Department of Electrical and Computer Engineering
Campus Box 425
Boulder, CO 80309-0425

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ABSTRACT *(Maximum 200 words)*

The first three months of this grant period have seen significant progress toward the project goals. A one bit optoelectronic counter has been constructed as a prototypical of an optoelectronic control unit. The counter runs at 305 MHz, and provided us much information on the timing and synchronization of such processors. We are beginning our work on developing or acquiring the optoelectronic integrated circuits and holographic optical elements that are necessary to the development of the optoelectronic graphic display processor, OGDP. We have also begun work on a CAD system for designing and constructing such processors. The CAD efforts have begun with development of algorithms for computint bit error rate in these systems We are also in the midst of developing the logical architecture for the OGDP, including control unit and front end processor design.

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An Optoelectronic Graphics Display Processor - OGDP

Vincent P. Heuring
June 14, 1993

Finite State Control Unit

A one-bit optoelectronic counter has been constructed and operated as prototypical of an optoelectronic control unit for controlling the optoelectronic graphics display processor, OGDP. This counter was built from optoelectronic NOR gates constructed from discrete components, and employed holographic optical elements for interconnection, as the final version of the OGDP control unit will. The NOR gates had rise and fall times of 150 and 200 ps respectively, fanout of 5, and gate latencies of .96 ns. Two synchronization mechanisms were used, gate-and-strobe, and time of flight. The counter employing the former synchronization mechanism ran at 120 MHz, and the latter ran at 305 MHz. This latter speed is very close to the calculated theoretical maximum, and is limited by the physical geometry of the system. A technical report describing the experiments above will be available at the end of the next reporting period.

OEICs

We are at the beginnings of our efforts to acquire or fabricate optoelectronic integrated circuits, OEICs. We are attacking this problem on several fronts, as we view it as being perhaps the central problem to be solved in developing an OGDP. We are discussing our requirements with personnel at Honeywell's Systems and Research Center in Bloomington MN. We are also exploring the possibility of having small prototypes fabricated by personnel here in the Optoelectronic Computing Systems Center. And last, we are studying the possibility of fabricating our own prototype devices using the MOSIS fabrication facilities.

Holographic Optical Elements

Several small holograms have been prepared by the OCS Center here, and were used in the one-bit counter described below. The Center has an active effort to fabricate HOEs, and we should be the beneficiaries of this work. In addition, we are participating in research to quantify the optical efficiency of HOEs prepared in various ways.

CAD System

The system we propose to design and construct is quite complex, both to visualize and to implement. We are constructing CAD tools to simplify both of these activities. The estimation of bit error rate as a function of detector and emitter characteristics and HOE properties is central to the CAD system. We have an active effort in this area, and will report preliminary results at the end of the next reporting period. We have also begun an effort to provide animated views of prospective machine architectures.

Algorithms

A technical report describing the graphics display processor architecture is being prepared. The report describes the instruction set of the processor, as well as the design of its control unit, and the interface to the front end processor.